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EXAMINER	
PERALTA, GINETTE	
ART UNIT	**PAPER NUMBER**
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,643	COMPAAN ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 29 recites the limitation "the transparent back layer" in line 5. There is insufficient antecedent basis for this limitation in the claim. It is understood by the examiner that it refers to the back electrode, but the back electrode is not characterized as being transparent.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 29 is rejected under 35 U.S.C. 102(b) as being anticipated by Matsuyama et al. (U. S. Pat. 5,714,010).

Matsuyama et al. discloses a method of making a diode structure like the one shown in Figs. 12(a) and 12(d) that comprises applying a back electrode coating layer *1202* to a polymer substrate (as disclosed in col. 19, lines 33-37, col. 51, lines 42-56); depositing an active semiconductor junction having a p-type layer *1205* and an n-type layer *1203* onto the back electrode *1202* under process conditions that avoid substantial degradation of the polymer substrate *1201*; and depositing a transparent electrode layer *1206* of CdO onto the semiconductor junction to form a diode structure.

5. Claims 35, 37, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Compaan et al. (U. S. Pat. 6,852,614 B1).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 35, Compaan et al. discloses a method of making a tandem diode structure that comprises depositing a first transparent front electrode layer *14* of any one of ZnO, ZnS and CdO onto a substrate layer *12*; depositing a first active semiconductor junction having an n-type layer *18* and a p-type layer *20* onto the first transparent electrode layer *14* under process conditions that avoid substantial degradation of the electrode layer *14*; depositing a first back transparent electrode

coating layer *22* under process conditions that avoid substantial degradation of the top electrode layer *14*, to form a first diode structure and to form a first layer of a tunnel junction; applying a second transparent front electrode coating layer *54* of any one of ZnO, ZnS and CdO onto the back transparent coating layer *22* of the top cell under process conditions that avoid substantial degradation of the top electrode layer *14*, with the second transparent electrode coating layer *54* completing the tunnel junction; depositing a second active semiconductor junction having an n-type layer *56* and a p-type layer *58* onto the second transparent electrode layer *54* under process conditions that avoid substantial degradation of both the first and second transparent electrode coating layers; and applying a second back electrode coating layer *60* to form a second diode structure and to complete the tandem diode structure as disclosed in Fig. 3 and in col. 6, lines 1-36, where the process conditions prevent the inclusion of copper in the process conditions in order to prevent the degradation of the electrode layers.

Regarding claim 37, Compaan et al. discloses that the deposition of one or both of the active semiconductor junctions is carried out with a sputtering process, as disclosed in col. 6, lines 54-56.

Regarding claim 38, Compaan et al. discloses in col. 6, lines 5-8 that one of the front electrode layers is ZnO doped with a Group III element.

Regarding claim 39, Compaan et al. discloses that the first back transparent electrode coating layer is ZnTe:N, as disclosed in col. 3, lines 65-67, and col. 6, lines 15-20.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 6-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oswald et al. (US Pat. Pub. 2003/0180983 A1) in view of Matsuyama et al. (U. S. Pat. 5,714,010)

Regarding claim 1, Oswald et al. discloses a method of making a diode structure that comprises depositing a transparent electrode layer *132* of ZnO onto a substrate layer *114* (as disclosed in ¶[0030]); depositing an active semiconductor junction *134* having an n-type layer and a p-type layer onto the transparent electrode layer *132* (as disclosed in ¶[0035]; and applying a back electrode coating layer *136* to form a diode structure (as disclosed in ¶[0038]).

Oswald et al. discloses the claimed invention with the exception of disclosing the process conditions under which the semiconductor layer is formed.

Matsuyama et al. discloses a method of making a diode structure as shown in Fig. 12(b) that comprises depositing a transparent electrode *1206* of CdO (among other materials) onto a substrate layer *1201;* depositing an active semiconductor junction

having an n-type layer *1203* and a p-type layer *1205* onto the transparent electrode layer *1206* under process conditions that avoid substantial degradation of the electrode layer, as taught in several modifications and variations disclosed in col. 53 line 36- col. 63, line 18, where various processes are disclosed for the deposition of an active semiconductor junction having an n-type layer and a p-type layer onto a transparent electrode layer for the purpose of not only avoiding substantial degradation of the electrode layer, but also for forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the active semiconductor junction of Oswald et al. by any of the disclosed methods of Matsuyama et al. for the disclosed intended purpose of forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Regarding claim 2, Oswald et al. as modified by Matsuyama et al. by implementing the deposition of an active semiconductor junction further discloses that

the depositing of the active semiconductor junction is carried out at a temperature less than about 400 degrees C, as disclosed in the embodiments taught in col. 54, lines 20-44 (Film Formation Example 1), col. 56, lines 58-67 (Film Formation Example 6), col. 57, lines 58-59 (Film Formation Example 7), among others. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the temperature as there is no statement denoting the criticality of the temperature, and all the temperature values taught by Matsuyama et al. lie within the claimed range of less than 400°C.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 3, Oswald et al. discloses that the active semiconductor junction may be deposited by a sputtering process in ¶[0035].

Regarding claim 4, Oswald et al. discloses that the active semiconductor junction may be carried out with one or more of an electro deposition process and a chemical bath deposition process as disclosed in ¶[0014] and [0035] (in the incorporation by reference of U. S. Pat. 5,472,910 and U. S. Pat. 4,064,521 among others cited.)

Regarding claim 6, Oswald et al. discloses in ¶[0015] and [0030] that the electrode layer comprises ZnO.

Regarding claim 7, Oswald et al. discloses in ¶[0015] that the ZnO is doped with a Group III element.

Regarding claim 8, Oswald et al. discloses in ¶[0015] that the ZnO is doped with aluminum.

Regarding claims 9 and 10, Oswald et al. as modified by Matsuyama et al. discloses that the layers of the active semiconductor junction are deposited in a manner limiting degradation of the ZnO transparent electrode layer to the extent that the electrical sheet resistance of the ZnO transparent layer is less than 10 ohms, and the transparency is greater than about 85% of visible light, as disclosed by Matsuyama et al. in col. 52, lines 34-37 and 55-61. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the electrical sheet resistance as there is no statement denoting the criticality of the electrical sheet resistance, and the desired electrical sheet resistance taught by Matsuyama et al. overlap with the claimed range of less than 5 ohms per square.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 11, Oswald et al. discloses that the diode structure is a thin-film photovoltaic cell as disclosed in ¶[0028].

Regarding claim 12, Oswald et al. as modified by Matsuyama et al. discloses that the diode structure is a thin film photovoltaic cell (as disclosed in ¶[0028] of Oswald et al.) and as modified by Matsuyama et al. the method results in a photovoltaic cell having a conversion efficiency greater than about 8 percent, as disclosed by Matsuyama et al. in col. 59, lines 62-67.

Regarding claim 13, Oswald et al. as modified by Matsuyama et al. discloses that the diode structure is a thin film photovoltaic cell (as disclosed in ¶[0028] of Oswald et al.) and as modified by Matsuyama et al. the method results in a photovoltaic cell having a conversion efficiency greater than about 10 percent, as disclosed by Matsuyama et al. in col. 61, lines 36-41.

Regarding claim 14, Oswald et al. discloses that the substrate may be glass having a conductive oxide already deposited thereon, thus teaching a superstrate, as disclosed in ¶[0030].

Regarding claim 15, Oswald et al. discloses a method of making a diode structure that comprises depositing a transparent electrode layer *132* of ZnO onto a substrate layer *114* which may be glass or plastic(as disclosed in ¶[0030]); depositing an active semiconductor junction *134* having an n-type layer and a p-type layer onto the transparent electrode layer *132* (as disclosed in ¶[0035]; and applying a back electrode coating layer *136* to form a diode structure (as disclosed in ¶[0038]).

Oswald et al. discloses the claimed invention with the exception of disclosing the process conditions under which the semiconductor layer is formed and specifying that the substrate is flexible.

Matsuyama et al. discloses a method of making a diode structure as shown in Fig. 12(b) that comprises depositing a transparent electrode *1206* of CdO (among other materials) onto a flexible substrate layer *1201;* depositing an active semiconductor junction having an n-type layer *1203* and a p-type layer *1205* onto the transparent electrode layer *1206* under process conditions that avoid substantial degradation of the electrode layer, as taught in several modifications and variations disclosed in col. 53 line 36- col. 63, line 18, where various processes are disclosed for the deposition of an active semiconductor junction having an n-type layer and a p-type layer onto a transparent electrode layer for the purpose of not only avoiding substantial degradation of the electrode layer, but also for forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the active semiconductor junction of Oswald et al. by any of the disclosed methods of Matsuyama et al. on a flexible substrate for the

disclosed intended purpose of forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Regarding claim 16, Oswald et al. as modified by Matsuyama et al. discloses that the flexible layer may be a polymer layer as disclosed by Matsuyama et al. in col. 19, lines 34-37.

Regarding claim 17, Oswald et al. as modified by Matsuyama et al. discloses that the flexible layer may be a metal film as disclosed by Matsuyama et al. in col. 9, lines 42-46.

Regarding claim 18, Oswald et al. discloses that the deposition of the active semiconductor junction is through a sputtering process carried out at a temperature less than 400 degrees as disclosed in ¶[0035] and its incorporation by reference of U. S. Pat. 4,064,521 as disclosed in ¶[0014]. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the temperature as there is no statement denoting the criticality of the temperature, and all the temperature values taught by Oswald et al. lie within the claimed range of less than 400°C.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16

USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 19, Oswald et al. discloses in ¶[0015] and [0030] that the electrode layer comprises ZnO and discloses in ¶[0015] that the ZnO is doped with a Group III element.

Regarding claim 20, Oswald et al. as modified by Matsuyama et al. discloses that the layers of the active semiconductor junction are deposited in a manner limiting degradation of the ZnO transparent electrode layer to the extent that the electrical sheet resistance of the ZnO transparent layer is less than 10 ohms, and the transparency is greater than about 85% of visible light, as disclosed by Matsuyama et al. in col. 52, lines 34-37 and 55-61. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the electrical sheet resistance as there is no statement denoting the criticality of the electrical sheet resistance, and the desired electrical sheet resistance taught by Matsuyama et al. overlap with the claimed range of less than 5 ohms per square.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 21, Oswald et al. as modified by Matsuyama et al. discloses that the diode structure is a thin film photovoltaic cell (as disclosed in ¶[0028] of Oswald et

al.) and as modified by Matsuyama et al. the method results in a photovoltaic cell having a conversion efficiency greater than about 8 percent, as disclosed by Matsuyama et al. in col. 59, lines 62-67.

Regarding claim 22, Oswald et al. as modified by Matsuyama et al. discloses that the diode structure is a thin film photovoltaic cell (as disclosed in ¶[0028] of Oswald et al.) and as modified by Matsuyama et al. the method results in a photovoltaic cell having a conversion efficiency greater than about 10 percent, as disclosed by Matsuyama et al. in col. 61, lines 36-41.

Regarding claim 23, Oswald et al. discloses a method of making a diode structure that comprises depositing a transparent electrode layer *132* of ZnO onto a substrate layer *114* (as disclosed in ¶[0030]); scribing the transparent electrode layer *132* into sections (as disclosed in ¶[0031]; depositing an active semiconductor junction *134* having an n-type layer and a p-type layer onto the transparent electrode layer *132* (as disclosed in ¶[0035]; scribing the active semiconductor junction *134* into sections (as disclosed in ¶[0036]; applying a back electrode coating layer *136* to form a diode structure (as disclosed in ¶[0038]); and scribing the back electrode coating layer *136* into sections (as disclosed in ¶[0039]); wherein a series of cells is formed, with each of the cells comprising one of the electrode layer sections *132*, one of the active semiconductor junction sections *134*; and one of the back electrode coating layer sections *136*, and wherein the series of cells is electrically connected in series to form a monolithically integrated solar panel, as shown in Fig. 3 and ¶[0058].

Oswald et al. discloses the claimed invention with the exception of disclosing the process conditions under which the semiconductor layer is formed and specifying that the substrate is flexible.

Matsuyama et al. discloses a method of making a diode structure as shown in Fig. 12(b) that comprises depositing a transparent electrode *1206* of CdO (among other materials) onto a flexible substrate layer *1201;* depositing an active semiconductor junction having an n-type layer *1203* and a p-type layer *1205* onto the transparent electrode layer *1206* under process conditions that avoid substantial degradation of the electrode layer, as taught in several modifications and variations disclosed in col. 53 line 36- col. 63, line 18, where various processes are disclosed for the deposition of an active semiconductor junction having an n-type layer and a p-type layer onto a transparent electrode layer for the purpose of not only avoiding substantial degradation of the electrode layer, but also for forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the active semiconductor junction of Oswald et al. by any of the disclosed methods of Matsuyama et al. on a flexible substrate for the

disclosed intended purpose of forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Regarding claim 24, Oswald et al. discloses in the incorporation by reference of U. S. Pat. 4,064,521 that the method for the deposition of the active junction includes sputtering at temperatures of less than 400°C, and Oswald et al. as modified by Matsuyama et al. further discloses by implementing the deposition of an active semiconductor junction discloses that the depositing of the active semiconductor junction is carried out at a temperature less than about 400 degrees C, as disclosed in the embodiments taught in col. 54, lines 20-44 (Film Formation Example 1), col. 56, lines 58-67 (Film Formation Example 6), col. 57, lines 58-59 (Film Formation Example 7), among others. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the temperature as there is no statement denoting the criticality of the temperature, and all the temperature values taught by Oswald et al. and Matsuyama et al. lie within the claimed range of less than 400°C.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim

was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 25, Oswald et al. discloses in ¶[0035] that the deposition of the active semiconductor junction may comprise a sputtering process.

Regarding claim 26, Oswald et al. discloses in ¶[0015] and [0030] that the electrode layer comprises ZnO and discloses in ¶[0015] that the ZnO is doped with a Group III element.

Regarding claim 27, Oswald et al. as modified by Matsuyama et al. discloses that the layers of the active semiconductor junction are deposited in a manner limiting degradation of the ZnO transparent electrode layer to the extent that the electrical sheet resistance of the ZnO transparent layer is less than 10 ohms, and the transparency is greater than about 85% of visible light, as disclosed by Matsuyama et al. in col. 52, lines 34-37 and 55-61. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the electrical sheet resistance as there is no statement denoting the criticality of the electrical sheet resistance, and the desired electrical sheet resistance taught by Matsuyama et al. overlap with the claimed range of less than 5 ohms per square.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 28, Oswald et al. as modified by Matsuyama et al. discloses that the diode structure is a thin film photovoltaic cell (as disclosed in ¶[0028] of Oswald et al.) and as modified by Matsuyama et al. the method results in a photovoltaic cell having a conversion efficiency greater than about 8 percent, as disclosed by Matsuyama et al. in col. 59, lines 62-67.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oswald et al. in view of Matsuyama et al. as applied to claims 1-4, 6-28 above, and further in view of Gordillo et al.'s *Influence of the Optical Window on the Performance of TCO/CdS/CdTe Solar Cells.*

Oswald et al. discloses a method of making a diode structure that comprises depositing a transparent electrode layer *132* of ZnO onto a substrate layer *114* (as disclosed in ¶[0030]); depositing an active semiconductor junction *134* having an n-type layer and a p-type layer onto the transparent electrode layer *132* (as disclosed in ¶[0035]; and applying a back electrode coating layer *136* to form a diode structure (as disclosed in ¶[0038]).

Oswald et al. discloses the claimed invention with the exception of disclosing the process conditions under which the semiconductor layer is formed and disclosing depositing the n-type layer carried out with a sputtering process, and depositing the p-type layer with one or more of electro deposition, a chemical bath deposition process, and a high temperature vapor deposition process.

Matsuyama et al. discloses a method of making a diode structure as shown in Fig. 12(b) that comprises depositing a transparent electrode *1206* of CdO (among other materials) onto a substrate layer *1201;* depositing an active semiconductor junction having an n-type layer *1203* and a p-type layer *1205* onto the transparent electrode layer *1206* under process conditions that avoid substantial degradation of the electrode layer, as taught in several modifications and variations disclosed in col. 53 line 36- col. 63, line 18, where various processes are disclosed for the deposition of an active semiconductor junction having an n-type layer and a p-type layer onto a transparent electrode layer for the purpose of not only avoiding substantial degradation of the electrode layer, but also for forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the active semiconductor junction of Oswald et al. by any of the disclosed methods of Matsuyama et al. for the disclosed intended purpose of forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a

desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Gordillo et al. discloses a method of making a diode structure that comprises depositing the n-type layer by a chemical bath deposition, and depositing a p-type layer by a high temperature bath deposition as disclosed in the abstract. Wherein Gordillo et al. discloses that two different methods may be used for the deposition of the n-type layer and the p-type layer for the disclosed intended purpose of growing a more homogeneous layer on the transparent electrode layer and improving the performance of the cell.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the methods of deposition of the various layers as long as the degradation of the transparent electrode layer is prevented, and for the disclosed intended purpose of growing a more homogeneous layer on the transparent electrode layer.

9. Claims 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuyama et al. in view of Oswald et al..

Matsuyama et al. discloses a method of making a diode structure like the one shown in Figs. 12(a) and 12(d) that comprises applying a back electrode coating layer *1202* to a polymer substrate (as disclosed in col. 19, lines 33-37, col. 51, lines 42-56); depositing an active semiconductor junction having a p-type layer *1205* and an n-type layer *1203* onto the back electrode *1202* under process conditions that avoid substantial

degradation of the polymer substrate *1201*; and depositing a transparent electrode layer *1206* of CdO onto the semiconductor junction to form a diode structure.

Regarding claim 30, Matsuyama et al. further discloses that the depositing of the active semiconductor junction is carried out at a temperature less than about 400 degrees C, as disclosed in the embodiments taught in col. 54, lines 20-44 (Film Formation Example 1), col. 56, lines 58-67 (Film Formation Example 6), col. 57, lines 58-59 (Film Formation Example 7), among others. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the temperature as there is no statement denoting the criticality of the temperature, and all the temperature values taught by Matsuyama et al. lie within the claimed range of less than 400°C.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 31, Matsuyama et al. discloses the claimed invention with the exception of depositing the active semiconductor junction by sputtering.

Oswald et al. discloses a method of making a diode structure that comprises depositing a transparent electrode layer *132* of ZnO onto a substrate layer *114* (as disclosed in ¶[0030]); depositing an active semiconductor junction *134* having an n-type layer and a p-type layer onto the transparent electrode layer *132* (as disclosed in

¶[0035]; and applying a back electrode coating layer *136* to form a diode structure (as disclosed in ¶[0038]) and further including that the active semiconductor junction may be deposited by a sputtering process as disclosed in ¶[0035], for the disclosed intended purpose of depositing the semiconductor junction by a well known process that results in a suitable semiconductor layer.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use various methods of deposition of the various layers as long as the degradation of the transparent electrode layer is prevented, and for the disclosed intended purpose of growing a suitable semiconductor layer useful in photovoltaic devices.

Regarding claim 32, Matsuyama et al. as modified by Oswald et al. discloses that ZnO, CdO, CdO_2SnO_2 and indium tin oxide can be used interchangeably as disclosed by Oswald et al. in ¶[0030] and by Matsuyama et al. in col. 52, lines 62-67. Furthermore, Oswald et al. discloses that the conductive oxide, in this case ZnO, may be doped with a Group III element, as disclosed in ¶[0015].

Regarding claim 33, Matsuyama et al. discloses that the layers of the active semiconductor junction are deposited in a manner limiting degradation of the transparent electrode layer to the extent that the electrical sheet resistance of the transparent layer is less than 10 ohms, and the transparency is greater than about 85% of visible light, as disclosed by Matsuyama et al. in col. 52, lines 34-37 and 55-61. Furthermore, it would have been obvious to one of ordinary skill in the art at the time

the invention was made to vary the electrical sheet resistance as there is no statement denoting the criticality of the electrical sheet resistance, and the desired electrical sheet resistance taught by Matsuyama et al. overlaps with the claimed range of less than 5 ohms per square.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 34, Matsuyama et al., as modified by Oswald et al., discloses that the diode structure is a thin film photovoltaic cell (as disclosed in ¶[0028] of Oswald et al.) and Matsuyama et al. further discloses that the method results in a photovoltaic cell having a conversion efficiency greater than about 8 percent, as disclosed in col. 59, lines 62-67.

10. Claim 36 is rejected under 35 U.S.C. 103(a) as being obvious over Compaan et al. in view of Matsuyama et al..

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject

matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Compaan et al. discloses a method of making a tandem diode structure that comprises depositing a first transparent front electrode layer *14* of any one of ZnO, ZnS and CdO onto a substrate layer *12*; depositing a first active semiconductor junction having an n-type layer *18* and a p-type layer *20* onto the first transparent electrode layer *14* under process conditions that avoid substantial degradation of the electrode layer *14*; depositing a first back transparent electrode coating layer *22* under process conditions that avoid substantial degradation of the top electrode layer *14*, to form a first diode structure and to form a first layer of a tunnel junction; applying a second transparent front electrode coating layer *54* of any one of ZnO, ZnS and CdO onto the back transparent coating layer *22* of the top cell under process conditions that avoid substantial degradation of the top electrode layer *14*, with the second transparent electrode coating layer *54* completing the tunnel junction; depositing a second active semiconductor junction having an n-type layer *56* and a p-type layer *58* onto the second

transparent electrode layer *54* under process conditions that avoid substantial degradation of both the first and second transparent electrode coating layers; and applying a second back electrode coating layer *60* to form a second diode structure and to complete the tandem diode structure as disclosed in Fig. 3 and in col. 6, lines 1-36, where the process conditions prevent the inclusion of copper in the process conditions in order to prevent the degradation of the electrode layers.

Compaan et al. discloses the claimed invention with the exception of disclosing the temperature or specific method by which the active semiconductor junction is deposited.

Matsuyama et al. discloses a method of making a diode structure like the one shown in Figs. 12(a) and 12(d) that comprises applying a back electrode coating layer *1202* to a polymer substrate (as disclosed in col. 19, lines 33-37, col. 51, lines 42-56); depositing an active semiconductor junction having a p-type layer *1205* and an n-type layer *1203* onto the back electrode *1202* under process conditions that avoid substantial degradation of the polymer substrate *1201*; and depositing a transparent electrode layer *1206* of CdO onto the semiconductor junction to form a diode structure. Matsuyama et al. further discloses that the depositing of the active semiconductor junction is carried out at a temperature less than about 400 degrees C, as disclosed in the embodiments taught in col. 54, lines 20-44 (Film Formation Example 1), col. 56, lines 58-67 (Film Formation Example 6), col. 57, lines 58-59 (Film Formation Example 7), among others.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a method such as the one described by Matsuyama et al. to deposit the active semiconductor junction of Compaan et al. for the disclosed intended purpose of forming a desirable high quality film having a uniform thickness and which stably exhibits the characteristics desired so that it is possible to mass-produce a multi-layered semiconductor device excelling in interface characteristics, and that stably exhibits a desirably high photoelectric conversion efficiency without deterioration even upon repeating use for a long period of time, as disclosed in col. 8,lines 25-49.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the temperature as there is no statement denoting the criticality of the temperature, and all the temperature values taught by Matsuyama et al. lie within the claimed range of less than 400°C.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

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PRIMARY EXAMINER